

I claim:

1. A circuit for determining a time difference between edges of a first digital signal and of a second digital signal, the circuit comprising:

a first input for receiving a first signal;

a plurality of basic elements connected in succession and in series, each one of said plurality of basic elements having an input, a control input, and a storage unit with an output, said plurality of basic elements including a first basic element having an input connected to said first input for receiving the first signal, said input of each one of said plurality of basic elements, except that of said first basic element, connected to said output of a respective preceding one of said plurality of basic elements;

a second input for receiving a second signal, said second input connected to said control input of each one of said plurality of basic elements; each one of said plurality of basic elements, except for said first basic element, configured such that if the second signal has a first level, said storage unit will store a signal level that is already stored in said storage unit of an immediately preceding one of said plurality of basic elements, and if the second signal has

a second level, said storage element will retain a previously stored signal level; and

a plurality of comparator units having outputs, each one of said plurality of comparator units receiving the signal level stored by said storage elements of two adjacent ones of said plurality of basic elements, each one of said plurality of comparator units supplying a different event signal at said output thereof when two identical signal levels are received from said storage elements of two adjacent ones of said plurality of basic elements than when two different signal levels are received.

2. The circuit according to claim 1, wherein each one of said plurality of basic elements includes a first switching unit connected in series with said storage element, said first switching unit of each one of said plurality of basic elements having a control input defining said control input of a respective one of said plurality of basic elements.

3. The circuit according to claim 1, wherein each one of said plurality of comparator units is an exclusive or gate.

4. The circuit according to claim 1, comprising:

a delay unit having an input for receiving a reference signal and having an output;

said delay unit including a plurality of delay elements connected in series, each one of said plurality of delay elements having an output;

said delay unit including a plurality of second switching units, each one of said plurality of second switching units configured between the output of a respective one of said plurality of delay elements and said output of the delay unit; and

each one of said plurality of second switching elements having a control input connected to the output of a respective one of said plurality of comparator units.

5. The circuit according to claim 1, wherein said storage unit of each one of said plurality of basic units includes two inverters connected antiparallel.

COMBINED DECLARATION AND POWER OF ATTORNEY  
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT FOR DETERMINING THE TIME DIFFERENCE BETWEEN EDGES OF A  
FIRST DIGITAL SIGNAL AND OF A SECOND DIGITAL SIGNAL

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 198 30 570.2, filed July 8, 1998, the International Priority of which is claimed under 35 U.S.C. §119; and International Application No. PCT/DE99/02008, filed July 1, 1999, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

HERBERT L. LERNER (Reg.No.20,435)  
LAURENCE A. GREENBERG (Reg.No.29,308)  
WERNER H. STEMER (Reg.No.34,956)  
RALPH E. LOCHER (Reg.No. 41,947)

Address all correspondence and telephone calls to:

LERNER AND GREENBERG, P.A.  
POST OFFICE BOX 2480  
HOLLYWOOD, FLORIDA 33022-2480  
TEL: (954) 925-1100 - FAX: (954) 925-1101

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE INVENTOR: MARTIN BUCK

INVENTOR'S SIGNATURE: \_\_\_\_\_

DATE: \_\_\_\_\_

Residence: MÜNCHEN, GERMANY

Country of Citizenship: GERMANY

Post Office Address: HOHENECKSTRASSE 28  
D-81243 MÜNCHEN  
GERMANY

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